Form PTO-1449 (Modified) Page 1 of 3	ATTY DOCKET NO. B-5138NP	U.S. SERIAL NO. 10/643,772
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS André DeHon, et al.	
	FILING DATE August 18, 2003	GROUP 2825

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUB-CLASS	FILING DATE or 102(e) DATE IF APPROPRIATE
W	5,144,563	9/1992	Date et al.	364	491	
W	5,796,625	8/1998	Scepanovic et al.	364	491	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

W	Alfke, P., "Efficient Shift Registers, LFSR Counters, and Long Psuedo-Random Sequence Generators," *Xilinx Application Note*, XAPP 052, INTERNET: <http://www.xilinx.com/xapp/xapp203.pdf> pp. 1-6 (July 7, 1996).
	Banerjee, P., *Parallel Algorithms for VLSI Computer-Aided Design*, Chapter 3, Englewood Cliffs, New Jersey: PTR Prentice Hall, pp. 118-171 (1994).
	Betz, V., et al., *Architecture and CAD for Deep-Submicron FPGAs*, Boston: Kluwer Acadmeic Publishers, pp. 50-61 (1999).
	Brelet, J., "An Overview of Multiple CAM Designs in Virtex Family Devices," *Xilinx Application Note*, XAPP201, INTERNET: <http://www.xilinx.com/xapp/xapp260.pdf> pp. 1-6 (September 23, 1999).
	Brelet, J., et al., "Designing Flexible, Fast CAMs with Virtex Family FPGAs," *Xilinx Application Note*, XAPP03, INTERNET: <http://www.xilinx.com/xapp/xapp203.pdf> pp. 1-17 (September 23, 1999).
	Caspi, E., et al., "Stream Computations Organized for Reconfigurable Execution (SCORE): Introduction and Tutorial," *presented at the Tenth International Conference on Field Programmable Logic and Applications*, Villach, Austria, INTERNET:<http://www.cs.berkeley.edu/projects/brass/documents/score_tutorial.html> 31 pages total (August 25, 2000).
	Chan, Pak K., et al., "Parallel Placement for Field-Programmable Gate Arrays," *presented at the Eleventh ACM International Symposium on Field-Programmable Gate Arrays*, Monterey, California, INTERNET: <http://www.doi.acm.org/10.1145/103724.103725> pp. 43-50 (2003).

EXAMINER	DATE CONSIDERED
[signature]	3/2/6

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Modified) Page 2 of 3	ATTY DOCKET NO. B-5138NP	U.S. SERIAL NO. 10/643,772
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS André DeHon, et al.	
	FILING DATE August 18, 2003	GROUP 2825

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

W	Chyan, Dah-Jun, et al., "A Placement Algorithm for Array Processors," *presented at the ACM/IEEE Design Automation Conference*, Miami Beach, Florida, INTERNET: <http://portal.acm.org/citation.cfm?id=800661> pp.182-188 (1983).
	Compton, K., et al., "Reconfigurable Computing: A Survey of Systems and Software," *ACM Computing Surveys (CSUR)*, Vol. 34, No. 2, INTERNET:<http://doi.acm.org/10.1145/508352.50353> pp.171-210 (June 2002).
	DeHon, A., et al., "Hardware-Assisted Fast Routing," *IEEE Symposium on Field-Programmable Custom Computing Machines*, Napa Valley, California, INTERNET: <http:www.cs.caltech.edu/research/ic/abstracts/fastroute_feem2002.html> pp. 1-11 (April 22-24, 2002).
	Goto, S., "An Efficient Algorithm for the Two-Dimensional Placement Problem in Electrical Circuit Design," *IEEE Transactions on Circuits and Systems*, Vol. CAS-28, No. 1, pp.12-18 (January 1981).
	Haldar, M., et al., "Parallel Algorithms for FPGA Placement," *Proceedings of the Tenth Great Lakes Symposium on VLSI*, INTERNET: <http://doi.acm.org/10.1145/330855.330988> pp.86-94 (2000).
	Huang, R., et al., "Stochastic, Spatial Routing for Hypergraphs, Trees, and Meshes," *Eleventh ACM International Symposium on Field-Programmable Gate Arrays*, INTERNET:<http://www.cs.caltech.edu/research/ic/abstracts/fastroute_fpga2003.html> 12 pages total (February 23-25, 2003).
	Kirkpatrick, S., et al., "Optimization by Stimulated Annealing," *Science*, Vol. 220, No. 4598, pp. 671-680 (May 13, 1983).
	Kravitz, S.A, et al., "Multiprocessor-Based Placement by Stimulated Annealing," *presented at the Twenty-Third IEEE Design Automation Conference*, Las Vegas, Nevada INTERNET: <http://doi.acm.org/10.1145/318013.318104> pp. 567-573 (1986)
	Mulpuri, C., et al., "Runtime and Quality Tradeoffs in FPGA Placement and Routing," *Proceedings of the Ninth International Symposium on Field-Programmable Gate Arrays*, INTERNET:<http://www.ee.washington.edu/faculty/hauck/publications/RuntimeTradeoffs.pdf> pp. 29-36 (February 11-13, 2001).

EXAMINER	DATE CONSIDERED
[signature]	3/2/6

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Modified) Page 3 of 3	ATTY DOCKET NO. B-5138NP	U.S. SERIAL NO. 10/643,772
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS André DeHon, et al.	
	FILING DATE August 18, 2003	GROUP 2825

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

V	Sankar, Y., et al., "Trading Quality for Compile Time: Ultra-Fast Placement for FPGAs," *Proceedings of the 1999 ACM/SIGDA Seventh International Symposium on Field Programmable Gate Arrays*, INTERNET:<http://www.eecg.toronto.edu/~jayar/pubs/sankar/fpga99sankar.pdf> pp. 157-166 (1999).
	Schnorr, C.P., et al., "An Optimal Sorting Algorithm For Mesh Connected Computers," *presented at the Eighteenth Annual ACM Symposium on Theory of Computing*, Berkeley, CA, INTERNET: <http://doi.acm.org/10.1145/359461.359481> pp. 255-270 (1986).
	Shahookar, K., et al., "VSLI Cell Placement Techniques," *ACM Computing Surveys (CSUR)*, Vol. 23, No. 2, pp.143-220 (June 1991).
	Spira, P., et al., "Hardware Acceleration of Gate Array Layout," *presented at the 22nd ACM/IEEE Design Automation Conference*, Las Vegas, Nevada, INTERNET: <http://doi.acm.org/10.1145/317825.317913> pp. 359-366 (1985).
	Tessier, R., "Fast Placement Approaches for FPGAs," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 7, No. 2 pp. 284-305, (April 2002).
	Thompson, C.D., et al., "Sorting on a Mesh-Connected Parallel Computer," *Communications of the ACM*, Vol. 20, No. 4, pp.263-271 (April 1977).

EXAMINER	DATE CONSIDERED
[signature]	3/26

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Modified) Page 1 of 3	ATTY DOCKET NO. B-5138NP 621881-3	U.S. SERIAL NO. 10/643,772
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS André DeHon, et al.	
	FILING DATE August 18, 2003	GROUP 2825

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUB-CLASS	FILING DATE or 102(e) DATE IF APPROPRIATE
W	3,654,615	4/1972	Freitag	340	172.5	
	5,495,419	2/1996	Rostoker et al.	364	468	
	6,243,851 B1	6/2001	Hwang et al.	716	10	
	2003/0174723 A1	9/2003	DeHon et al.	370	404	
	2005/0063373 A1	3/2005	DeHon et al.	370	380	

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO
WD	98/35294	8/1998	WO			abstract

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

WD	Arora, S., et al., "On-Line Algorithms For Path Selection In A Nonblocking Network," *SIAM Journal on Computing*, Vol. 25, No. 3, pp. 1-25 (June 1996).
WD	Banerjee, P., et al., "A Parallel Simulated Annealing Algorithm for Standard Cell Placement on a Hypercube Computer," *IEEE International Conference on Computer-Aided Design*, pp. 34-37 (1986).
WD	Banerjee, P., et al., "Parallel Simulated Annealing Algorithms for Cell Placement on Hypercube Multiprocessors," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 1, No. 1, pp. 91-106 (1990).
WD	Bhatt, S.N., et al., "A Framework for Solving VLSI Graph Layout Problems," *Journal of Computer and System Sciences*, Vol. 28, pp. 300-345 (1984).
WD	Chan, P.K., et al., "Acceleration of an FPGA Router," *Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, IEEE*, pp. 175-181 (April 1997).
WD	Chan, P.K., et al., "New Parallelization and Convergence Results for NC: A Negotiation-Based FPGA Router," *Proceedings of the 2000 International Symposium on Field-Programmable Gate Arrays (FPGA '00), ACM/SIGDA*, pp 165-174 (February 2000).
	Chong, F., et al., "METRO: A Router Architecture for High-Performance, Short-Haul Routing Networks," *Proceedings of the Annual International Symposium on Computer Architecture, Chicago, IEEE*, Vol. SYMP. 21, pp 266-277 (April 18-21, 1994).

EXAMINER	DATE CONSIDERED
	3/21/06

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Modified) Page 2 of 3	ATTY DOCKET NO. B-5138NP 621881-3	U.S. SERIAL NO. 10/643,772
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS André DeHon, et al.	
	FILING DATE August 18, 2003	GROUP 2825

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

WD	Dally, W.J., "Express Cubes: Improving the Performance of *k*-ary *n*-cube Interconnection Networks," *IEEE Transactions on Computers*, Vol. 40, No. 9, pp. 1016-1023 (September 1991).
WD	DeHon, A., "Balancing Interconnect and Computation in a Reconfigurable Computing Array (or why you don't really want 100% LUT utilization)," *Proceedings of the 1999 ACM/SGDA Seventh International Symposium on Field Programmable Gate Arrays*, pp. 1-10 (February 21-23, 1999).
WD	DeHon, A., "Compact, Multilayer Layout for Butterfly Fat-Tree," *Proceedings of the Twelfth ACM Symposium on Parallel Algorithms and Architectures*, 10 pages total (July 2000).
WD	DeHon, A., "Entropy, Counting and Programmable Interconnect," *FPGA'96, ACM-SIGDA Fourth International Symposium on FPGAs*, Monterey CA, Fig. 2, 7 pages total (February 11-13 1996).
WD	DeHon, A., "Rent's Rule Based Switching Requirements, System Level Interconnect Prediction," *SLIP 2001*, pp. 197-204 (March 31-April 1, 2001).
WD	Erényi, I., et al., "FPGA-based Fine Grain Processor Array Design Considerations," Proceedings of the Third IEEE International Conference, pp. 659-662 (1996).
WD	Fiduccia, C.M., et al., "A Linear-Time Heuristic for Improving Network Partitions," *19th Design Automation Conference*, Paper 13.1, pp. 175-181 (1982).
WD	Greenberg, R.I., et al., "A Compact Layout for the Three-Dimensional Tree of Meshes," *Appl. Math. Lett.*, Vol. 1, No. 2, pp. 171-176 (1988).
WD	Greenberg, R.I., et al., "Randomized Routing on Fat-Trees," *Laboratory for Computer Science, Massachusetts Institute of Technology*, Cambridge, Massachusetts, pp. 1-23 (June 13, 1996).
WD	Henry, D.S., et al., "Cyclic Segmented Parallel Prefix," *Ultrascalar Memo 1*, Yale, pp. 1-14 (November 1998).
WD	Horvath, E.I, "A Parallel Porce Direct Based VLSI Standard Cell Placement Algorithm," *Proceedings of the International Symposium on Circuits and Systems*, Vol. 2, pp. 2071-2074 (1993).
WD	Iosupovici, A., "A Class of Array Architectures for Hardware Grid Routers," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. CAD-5, No. 2, pp. 245-255 (April 1986).
WD	Kernighan, B.W., et al., "An Efficient Heuristic Procedure for Partitioning Graphs," *Bell Syst. Tech. J.*, Vol. 49, No. 2, pp. 76-80 (February 1970).
WD	Landman, B.S., et al., "On Pin Versus Block Relationship for Partitions of Logic Graphs," *IEEE Transactions on Computers*, Vol. C-20, No. 12, pp. 1469-1479 (1971).

EXAMINER	DATE CONSIDERED
[signature]	7/26

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Modified) Page 3 of 3	ATTY DOCKET NO. B-5138NP 621881-3	U.S. SERIAL NO. 10/643,772
LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS André DeHon, et al.	
	FILING DATE August 18, 2003	GROUP 2825

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

WD	Leiserson, C.E., "Fat Trees: Universal Networks for Hardware-Efficient Supercomputing," *IEEE Transactions on Computers*, Vol.C-34, No. 10, pp. 892-901 (October 1985).
WD	McMurchie, L., et al., "PathFinder: A Negotiation-Based Performance-Driven Router for FPGAs," *Proceedings of the ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, ACM*, pp. 111-117 (February 1995).
WD	"METIS: Family of Multilevel Partitioning Algorithms," INTERNET: <http://www-users.cs.umn.edu/~karypis/metis/index.html> 1 page total (Retrieved on February 4, 2005).
WD	Ryan, T., et al., "An ISMA Lee Router Accelerator," *IEEE Design and Test of Computers*, pp 38-45 (October 1987).
WD	Sai-Halasz, G.A., "Performance Trends in High-End Processors," *Proceedings of the IEEE*, Vol. 83, No. 1, pp. 20-36 (January 1995).
WD	"SS7 Tutorial," *Performance Technologies*, INTERNET: <http://www.pt.com/tutorials/ss7> pp. 1-23 (August 22, 2001).
WD	Swartz, J.S., et al., "A Fast Routability-Driven Router for FPGAs," *Proceedings of the 1998 International Symposium on Field-Programmable Gate Arrays (FPGA '98)*, pp. 140-149 (February 1998).
WD	Tessier, R., "Negotiated A* Routing for FPGAs," *Proceedings of the 5th Canadian Workshop on Field Programmable Devices*, 6 pages total (June 1998).
WD	Thompson, C.D., "Area-Time Complexity for VLSI," *Eleventh Annual ACM Symposium on Theory of Computing*, pp. 81-88 (May 1979).
WD	Togawa, N., et al., "An Incremental Placement and Global Routing Algorithm for Field-Programmable Gate Arrays," *Design Automation Conference*, pp. 519-526 (1998).
WD	Togawa, N., et al., "Maple: A Simultaneous Technology Mapping, Placement, and Global Routing Algorithm for Field-Programmable Gate Arrays," *IEEE/ACM International Conference on Computer-Aided Design*, pp. 156-163 (1994).
WD	Tsu, W., et al., "HSRA: High-Speed, Hierarchical Synchronous Reconfigurable Array," *Proceedings of the International Symposium on Field Programmable Gate Arrays*, pp 1-10 (February 1999).
WD	Wu, Yu-Liang, et al., "Graph-Based Analysis of 2-D FPGA Routing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 1, pp. 33-44 (January 1996).

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.